WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a memory cell array including a plurality of memory cells each connected to one of a plurality of bit lines and one of a plurality of word lines;

sense amplifiers for amplifying a small potential difference read from said memory cell array to said bit lines;

control means for controlling reading of data from said memory cell array and writing of data to said memory cell array; and

potential setting means for setting low level potential lines of said bit lines, said memory cells and said sense amplifiers to a potential higher than low level of said word lines.

2. The semiconductor memory device according to claim 1, wherein

said potential setting means includes a first semiconductor element for elevating the potential of said low level potential line by its threshold voltage.

3. The semiconductor memory device according to claim 2, wherein

said potential setting means includes a second semiconductor element connected parallel to said first semiconductor element, rendered conductive in response to a signal corresponding to a period in which a large current flows, for discharging the potential of said low level potential line.

4. The semiconductor memory device according to claim 3, wherein

said potential setting means includes

reference voltage generating means for generating a reference voltage which is approximately equal to said low level potential, and

potential compensating means for comparing said low level potential line with the reference voltage generated from said reference voltage generating means, and for elevating the potential of said low level potential line to a potential higher than low level of said word lines.

5. The semiconductor memory device according to claim 4, wherein

said potential compensating means includes

comparing means comparing the potential of said low level potential line and said reference voltage, and

switching means responsive to a comparison output

from said comparing means for supplying a potential of a power supply line to the line of said low level potential so as to set the low level potential line to a potential higher than low level of said word lines.

6. The semiconductor memory device according to claim 3, wherein

said potential setting means includes sustain means for intermittently supplying a power supply potential to low level potential line so as to set the potential of the line to a level higher than low level of said word lines.

7. The semiconductor memory device according to claim 6, wherein

said sustain means includes

an intermittently oscillating oscillation circuit, and

a pumping circuit responsive to oscillation output from said oscillation circuit for supplying said power supply voltage to low level potential line.

8. The semiconductor memory device according to claim 1, wherein

said potential setting means includes

reference voltage generating means for generating a

reference voltage which is approximately equal to the potential of said low level potential line,

comparing means for comparing the reference voltage from said reference voltage generating means and the potential of said low level potential line, and

switching means responsive to a comparison output from said comparing means for discharging the potential of said low level potential line to low level of said word lines.

9. The semiconductor memory device according to claim 8, further comprising:

level lowering preventing means connected between said switching means and said low level potential line for preventing lowering of the potential of said low level potential line from that potential which is higher than low level of said word lines.

10. The semiconductor memory device according to claim 9, wherein

said level lowering preventing means includes a diode.

11. The semiconductor memory device according to claim 10, further comprising:

a decoupling capacitor connected between a node between said switching means and said diode and low level of said word lines, for absorbing change in potential.

12. The semiconductor memory device according to claim 8, further comprising:

voltage comparison stopping means responsive to a signal corresponding to a period in which a large current flows, for disabling said voltage comparing means; and

float preventing means responsive to said signal corresponding to the period in which the large current flows for forcing said switching means to operate to prevent floating of the potential of said low level potential line.

13. The semiconductor memory device according to claim 1, wherein

each said sense amplifier includes a switching element connected between the low level potential line and the ground for elevating the potential of said low level potential line by its threshold voltage.

14. The semiconductor memory device according to claim 13, wherein

said switching element includes an element which is

rendered conductive in response to the signal which corresponds to a period in which large current flows.

15. The semiconductor memory device according to claim 14, wherein

said switching element is rendered conductive when its input electrode falls to a potential not higher than low level of said word lines;

said semiconductor memory device further comprising:

negative potential voltage generating means for generating a voltage of negative potential, and

switching means responsive to said signal corresponding to a period in which large current flows for applying the negative potential voltage generated from said negative potential voltage generating means only in said period to the input electrode of said switching element so as to make response time shorter.

16. The semiconductor memory device according to claim 15, wherein

said switching means includes means for supplying, in a former half of said period corresponding to a period in which the large current flows, low level of said word lines to the input electrode of said switching element, and in a former half period, said negative potential to

the input electrode of said switching element.

17. The semiconductor memory device according to claim 1, further comprising:

word line driving means for driving said word lines, and

switching means for switching a low level potential line of said word line driving means to the ground or to an output of said potential setting means.

18. The semiconductor memory device according to claim 17, wherein

said switching means includes means for switching said line from low level of said word lines to said output of said potential setting means before said word line rises from a first logic to a second logic.

19. The semiconductor memory device according to claim 17, wherein

said memory cell array is arranged in a plurality of blocks, and

said switching means includes means for switching said line from low level of said word lines to said output of said potential setting means before said word line rises from a first logic to a second logic in each said block.

20. The semiconductor memory device according to claim 19, wherein

said switching means includes means for switching a non-selected word line from the output of said potential setting means to low level of said word lines, after a selected word line rises from the first logic to the second logic in each said block.

21. A semiconductor memory device, comprising;

a memory cell array including memory cells each connected to one of a plurality of bit lines and one of a plurality of word lines;

sense amplifiers for amplifying a small potential difference read from said memory cell array to said bit line;

control means for controlling reading of data from said memory cell array and writing of data to said memory cell array;

potential setting means for setting low level potential lines of said bit lines, said memory cells and said sense amplifiers to a potential higher than low level of said word lines;

potential elevating compensating means responsive to lowering of said potential set higher than low level of

said word lines by said potential setting means for elevating the potential for compensation; and

potential lowering compensating means responsive to a rise of said potential set higher than low level of said word lines by said potential setting means for lowering the potential for compensation.

22. A semiconductor memory device, comprising:

a memory cell array including memory cells each connected to one of a plurality of bit lines and one of a plurality of word lines;

a sense amplifier for amplifying a small potential difference read from said memory cell array to said bit lines;

control means for controlling reading of data from said memory cell array and writing of data to said memory cell array;

a drive line for driving said sense amplifier; and

potential setting means for setting, when said sense amplifier is driven, a low level potential of said sense amplifier drive line to a potential higher than low level of said word lines.

23. The semiconductor memory device according to claim 22, wherein

said potential setting means includes means for setting said sense amplifier drive line at a potential higher than low level of said word lines and lower than a precharge level of said bit lines.

24. The semiconductor memory device according to claim 22, wherein

said potential setting means includes means for setting said sense amplifier drive line to a level higher than a level when said word line is not selected.

25. The semiconductor memory device according to claim 22, wherein

said potential setting means includes

potential generating means for generating a potential higher than low level of said word lines, and

a semiconductor element for supplying, when said sense amplifier is driven, the potential generated from said potential generating means to said sense amplifier drive line.

26. The semiconductor memory device according to claim 22, wherein

said potential setting means includes

first potential forcing means for forcing, in an

initial period of driving said sense amplifier, said sense amplifier drive line to low level of said word lines, and

second potential forcing means for forcing, after a lapse of the initial period of driving said sense amplifier, said sense amplifier drive line to a potential higher than low level of said word lines.

27. The semiconductor memory device according to claim 26, wherein

said second potential forcing means includes

a potential generating circuit for generating a voltage higher than low level of said word lines, and

a first semiconductor element for supplying the voltage provided by said potential generating circuit to said sense amplifier drive line.

28. The semiconductor memory device according to claim 26, wherein

said second potential forcing means includes

a second semiconductor element which is rendered conductive after the lapse of the initial period of driving said sense amplifier, and

a transistor element diode-connected between said second semiconductor element and the ground.

29. The semiconductor memory device according to claim 22, wherein

said potential setting means includes

comparing means for comparing, when said sense amplifier is driven, voltage of said sense amplifier drive line with a predetermined reference voltage, and

a first semiconductor element responsive to a comparison output from said comparing means for discharging low level potential of said sense amplifier driven line to a potential higher than low level of said word lines.

30. The semiconductor memory device according to claim 29, further comprising:

a second semiconductor element for forcing, when said sense amplifier is not driven, said first semiconductor element to be non-conductive.

31. The semiconductor memory device according to claim 29, further comprising

level conversion means for converting the level of the voltage of said sense amplifier drive line and for applying it to said comparing means as a comparison input.

32. The semiconductor memory device according to

claim 29, wherein

said comparing means includes means for applying a negative potential voltage to said first semiconductor element when said sense amplifier is not driven.

33. The semiconductor memory device according to claim 30, wherein

said comparing means includes a current comparing circuit.

34. The semiconductor memory device according to claim 33, wherein

said current comparing circuit includes hysteresis control means for adapting a reference level to have hysteresis characteristic.

35. The semiconductor memory device according to claim 22, further comprising:

a test circuit for testing data retention time of said memory cell; and

low level of said word lines forcing means for forcing, when said memory cell is tested by said test circuit, said sense amplifier drive line to the low level of said word lines.

36. The semiconductor memory device according to claim 22, wherein

said memory cell arrays is arranged in a plurality of blocks, and

said potential setting means is provided for each block.

37. A semiconductor memory device, comprising:

a memory cell array including memory cells each connected to one of a plurality of bit lines and one of a plurality of word lines;

a sense amplifier for amplifying a small potential difference read from said memory array to said bit lines;

a transfer gate connected between said bit lines and said sense amplifier; and

control means for controlling, when said sense amplifier is driven, gate potential of said transfer gate such that the gate potential is set to low level of said word lines, and a low level potential of said bit lines such that the low level potential is made higher by a threshold voltage of said transfer gate.

38. The semiconductor memory device according to claim 37, wherein

said control means includes switching means for

switching the low level potential of said bit lines when said sense amplifier is driven to a potential higher than the low level potential of said sense amplifier.

39. The semiconductor memory device according to claim 37, wherein

said control means includes switching means for switching a low level potential of said sense amplifier such that the low level potential when said sense amplifier is driven is made higher than the low level potential of said bit lines before completion of said sense amplifier drive.

40. The semiconductor memory device according to claim 37, further comprising

a drive line for driving said sense amplifier; wherein

said switching means includes means for connecting, at the start of driving of said sense amplifier, the drive line of said sense amplifier to low level of said word lines, and after initial sensing operation, switching said drive line to a potential higher than low level of said word lines.

41. A semiconductor memory device, comprising:

a memory cell array including memory cells each connected to one of a plurality of bit lines and one of a plurality of word lines;

a sense amplifier for amplifying a small potential difference read from said memory cell array to said bit lines;

control means for controlling reading of data from said memory cell array and writing of data to said memory cell array; and

potential setting means for setting low level potential lines of said bit lines, said memory cells and said sense amplifier to a potential higher than low level of said word lines, and for setting a high level potential at a potential lower than an externally applied power supply voltage.

42. The semiconductor memory device according to claim 41, wherein

said potential setting means includes means for setting said low level potential and said high level potential to arbitrary potentials, respectively.

43. The semiconductor memory device according to claim 42, wherein

said potential setting means includes means for

arbitrarily setting said low level potential and said high level potential, while maintaining constant potential difference between said low level potential and said high level potential.

44. The semiconductor memory device according to claim 41, wherein

said potential setting means includes

high level potential setting means for setting said high level potential based on a first reference potential, and

a low level potential setting means for setting said low level potential based on a second reference potential.

45. The semiconductor memory device according to claim 44, further comprising:

reference potential generating means for generating said first and said second reference potentials.

46. The semiconductor memory device according to claim 45, wherein

said reference potential generating means includes means for generating said first and second reference potentials while maintaining constant level difference between the first and the second reference potentials.

47. The semiconductor memory device according to claim 41, wherein

said potential setting means includes switching means for switching said low level potential to a potential approximately equal to low level of said word lines for only a predetermined period.

48. The semiconductor memory device according to claim 41, wherein

said potential setting means includes

a plurality of first resistors connected in parallel each for setting said first reference potential to an arbitrary potential,

a plurality of first fuses connected in series corresponding to said plurality of first resistors, invalidating corresponding one of the first resistors when blown off, and

a plurality of second resistors connected in parallel each for setting said second reference potential to an arbitrary potential, and

a plurality of second fuses connected in series corresponding to said plurality of second resistors, invalidating corresponding one of the second resistors when blown off.

49. The semiconductor memory device according to claim 48, further comprising

a plurality of transistors connected in series to said plurality of first and second fuses for rendering conductive or non-conductive the first and the second fuses for adjusting said first and second reference potentials.

50. A semiconductor memory device having an internal circuit to which a power supply voltage is externally applied, comprising:

potential setting means for setting a high level potential supplied to said internal circuit to a potential different from said externally supplied power supply voltage, and for setting a low level potential supplied to said internal circuit to a potential different from low level of said word lines, and

means for changing the high level potential and the low level potential set by said potential setting means dependent on whether semiconductor memory device is in use or not in use.

51. A semiconductor memory device having a chip formed on a semiconductor substrate, comprising:

a memory cell array including memory cells each connected to one of a plurality of bit lines and one of a plurality of word lines;

a sense amplifier for amplifying a small potential difference read from said memory cell array to the bit lines;

control means for controlling reading of data from said memory cell array and writing of data to said memory cell array;

substrate potential generating means for supplying a negative level substrate potential to said semiconductor substrate;

boosted voltage generating means for generating a boosted voltage to be supplied to said word lines; and

potential setting means for switching potential of said boosted voltage and said negative level potential to arbitrary potentials dependent on whether the chip is in use or not in use.

52. A semiconductor memory device, comprising:

a memory cell array including a plurality of memory cells each connected to one of a plurality of bit lines and one of a plurality of word lines;

a sense amplifier for amplifying a small potential difference read from said memory cell array to said bit

lines;

control means for controlling reading of data from said memory cell array and writing of data to said memory cell array;

potential setting means for setting low level potential lines of said bit lines, said memory cells and said sense amplifier to a potential higher than low level of said word lines, and

potential compensating means for compensating the low level potential set by said potential setting means.

53. A semiconductor memory device having a chip formed on a semiconductor substrate, comprising:

a memory cell array including memory cells each connected to one of a plurality of bit lines and one of a plurality of word lines;

a sense amplifier for amplifying a small potential difference read from said memory cell array to the bit lines;

control means for controlling reading of data from said memory cell array and writing of data to said memory cell array;

potential setting means for setting low level potential lines of said bit lines, said memory cells and said sense amplifier to a potential higher than low level

of said word lines; and

low level of said word lines forcing means for forcing, when data retention time of said memory cells is tested, the low level potential lines of said bit lines, said memory cells and said amplifier to low level of said word lines.

54. The semiconductor memory device according to claim 53, further comprising:

word line driving means for driving said word lines; and

switching means for switching, when data retention time of said memory cells is tested, the low level potential line of said word line driving means from ground side to a side of an output of said potential setting means.

55. A semiconductor memory device having a chip formed on a semiconductor substrate, comprising:

a memory cell array including a plurality of memory cells each connected to one of a plurality of bit lines and one of a plurality of word lines;

word line driving means for driving said word lines;

a sense amplifier for amplifying a small potential difference read from said memory cell array to the bit

lines;

control means for controlling reading of data from said memory cell array and writing data to said memory cell array; and

potential setting means for setting, when data retention time of said memory cells is tested, low level potential line of said word line driving means to a potential higher than low level of said word lines.

56. The semiconductor memory device according to claim 55, further comprising:

substrate potential generating means for generating a negative level substrate potential to said semiconductor substrate; and

substrate potential setting means for setting, when data retention time of said memory cells is tested, the substrate potential of said semiconductor substrate higher than said negative level substrate potential.

57. A semiconductor memory device having a chip formed on a semiconductor substrate, comprising:

a memory cell array including memory cells each connected to one of a plurality of bit lines and one of a plurality of word lines;

a sense amplifier for amplifying a small potential

difference read from said memory cell array to the bit lines;

control means for controlling reading of data from said memory cell array and writing of data to said memory cell array;

substrate potential generating means for supplying a negative level substrate potential to said semiconductor substrate; and

substrate potential setting means for setting, when data retention time of said memory cells is tested, the substrate potential of said semiconductor substrate higher than said negative level substrate potential.